

ARMY RESEARCH LABORATORY



## **Three Dimensional Packaging of Very Large Scale Integrated Optics (VLSIO) for High Complexity Optical Systems**

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13. ABSTRACT (Maximum 200 words) Optics has the fundamental capability of dramatically improving computer performance via the reduction of capacitance for intrinsic high bandwidth communications and low power usage. Yet optical devices have not displaced silicon VLSI in any measure to date. The reason is clear. When placed into systems, the optical devices have not had significantly greater performance in equally complex information processing circuits and similarly low manufacturing cost. An approach demonstrated here used the same system integration techniques that have been successful for silicon electronics, only applied to optics. Essential for creation of Very Large Scale Integrated Optics (VLSIO), with over 50,000 high speed logic gates per sq cm, is a new class of Ultra High Confinement (UHC) waveguides. These waveguides are created with high index difference (as high as 4.0 to 1.0) between guide and cladding. The waveguides have been demonstrated with infrared cross sections less than 5% of a square free space wavelength. These waveguides can be manufactured today only in the mid-infrared, but the concepts should scale to the near-infrared as lithography improves. Waveguide corners have been designed and demonstrated with a bend radius of less than one free space wavelength. Resonators have been designed which have over 100 times smaller volume than vertical cavity surface emitting lasers (VCSELs), yet efficiently interconnected laterally in high densities. A connector to the UHC waveguides has been developed and demonstrated using diffractive optical element arrays on the back side of the substrate. The coupler arrays can allow up to 10,000 Gaussian beam connections per sq cm. The connectivity also has advantages for low cost three-dimensional packaging for reduced cost and thermal dissipation. Experimental results on the above concepts and components are presented.				
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# Three Dimensional Packaging of Very Large Scale Integrated Optics (VLSIO) for High Complexity Optical Systems

## 1. INTRODUCTION

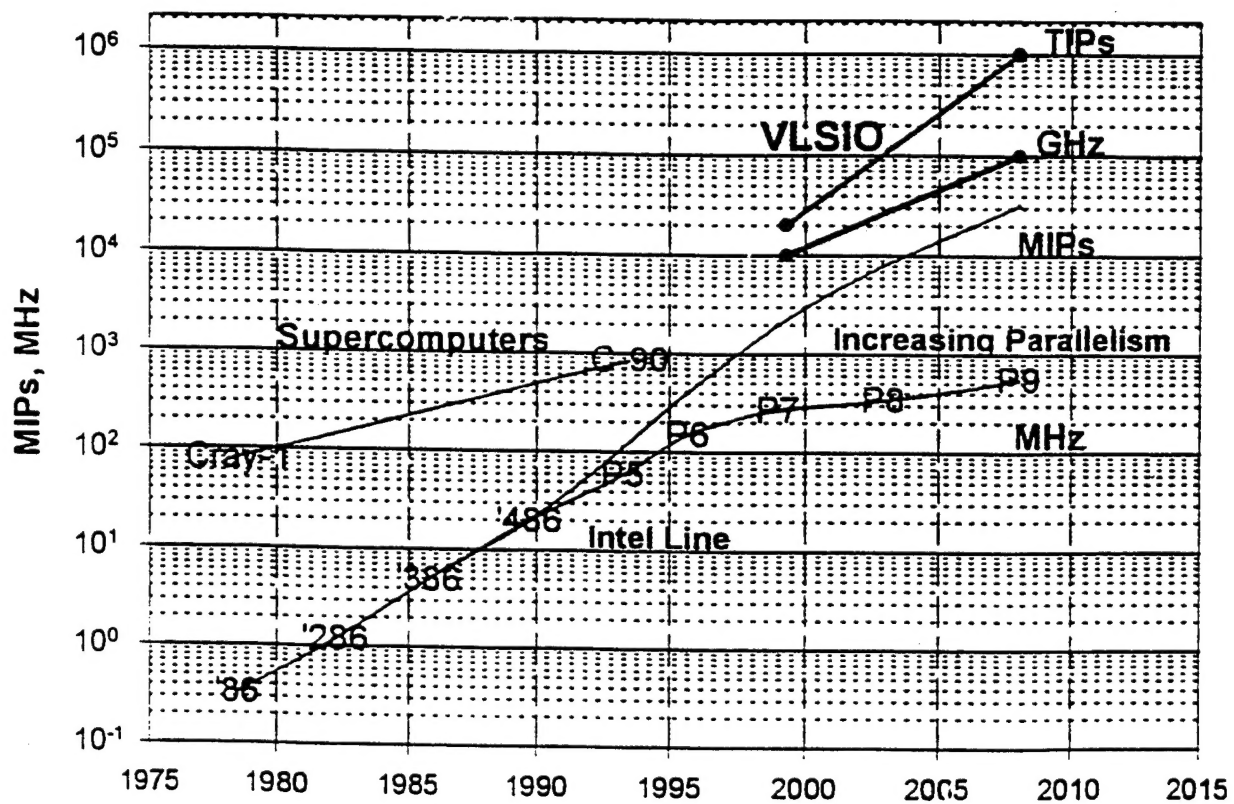
Optics has the fundamental capability of dramatically improving computer performance via the reduction of capacitance for intrinsic high bandwidth communications and low power usage. Yet optical devices have not displaced silicon VLSI in any measure to date. The reason is clear. When placed into systems, the optical devices have not had significantly greater performance in equally complex information processing circuits and similarly low manufacturing cost.

An approach demonstrated here uses the same system integration techniques that have been successful for silicon electronics, only applied to optics. Essential for creation of Very Large Scale Integrated Optics (VLSIO), with over 50,000 high speed logic gates per square centimeter, is a new class of Ultra High Confinement (UHC) waveguides. These waveguides are created with high index difference (as high as 4.0 to 1.0) between guide and cladding. The waveguides have been demonstrated with infrared cross sections less than 5% of a square free space wavelength. These waveguides can be manufactured today only in the mid-infrared, but the concepts should scale to the near-infrared as lithography improves. Waveguide corners have been designed and demonstrated with a bend radius of less than one free space wavelength. Resonators have been designed which have over 100 times smaller volume than VCSELs, yet efficiently interconnected laterally in high densities. A connector to the UHC waveguides has been developed and demonstrated using diffractive optical element arrays on the back side of the substrate. The coupler arrays can allow up to 10,000 Gaussian beam connections per square centimeter. This connectivity also has advantages for low cost three dimensional packaging for reduced cost and thermal dissipation. Experimental results on the above concepts and components will be presented.

## 2. MOTIVATION

### 2.1 Modern computing power is a result of production power.

The most impressive example of manufacturing technology in the information age is that of VLSI electronics. From the view of an individual in use of computing power, it would appear that computers have become two times faster every two years, with over a thousandfold performance increase during the last 20 years. However, this phenomenon has not been so much a result of advancement in transistors, but rather in the manufacture of systems. Computers have simply become less expensive every year, allowing the customer to purchase more power every year. Individual logic gates upon which the computer systems are based have become faster, but only in proportion to the decreasing lithographic linewidths. This tenfold improvement in electronic logic gate speed over the last 20 years, as a result of manufacturing size improvements, is only a small part of the thousandfold gains seen by the consumer, which is mostly from greater affordability. This is not just a point of view, but an important statement on the limits of computing advances. For if computers were simply getting faster, equal advances in computing power should occur from personal computers to supercomputers. However, as can be seen from Figure 1, there has been a convergence such that supercomputers, workstations, and high performance personal computers are all now within a factor of five of each other in performance, compared to the 10,000 ratio in performance that existed 20 years ago. Supercomputers have only improved by a small factor, only slightly greater than the improvement in logic gate speed. This convergence in computer performance illustrates that computer power cannot be easily improved, even for great increases in price. Over the past 20 years, most all gains in the computer revolution have been in manufacturing and price. The resulting expansion of computing has been a great benefit to society, but individual computer technology has not greatly improved.



**Figure 1.** Serial Speed for Pcs and Supercomputers with Projections for Very Large Scale Integrated Optical Computers. The clock frequency for electronic systems peaks at around 1,000 MHz, further gains are from parallelism.

## 2.2 Computer architectures have strong diminishing returns after 150,000 logic gates.

Furthermore, up to now, improvements in integration levels that arose from the manufacturing improvements could be used to directly advance the computer power in proportion to the improvements in integration level. The architecture could simply incorporate more concepts already proven in supercomputer technologies. However, serial supercomputers reach a rapidly diminishing return in performance with increasing logic counts beyond about 150,000 logic gates. The Intel Pentium with about 3 million transistors has approximately this number of logic gates, with the majority of transistors used for cache memory. At this level of complexity, one can perform instruction pre-fetch, decode, and execution, pipelined floating point conversions and math, conditional branch prediction, and other proven concepts for performance. With increases in gate count beyond this level, one can use the gates to create multiple pipelines, speculative execution along several branches with the wrong branches discarded, and hardware implementations of important math functions. But the increase in program performance from these extensions no longer improves in proportion to the number of logic gates.<sup>1</sup> Similarly, parallel computing concepts also have decreasing efficiencies with increasing integration levels, except for very specialized applications. The recent convergence in serial computer speeds is a result of the rapidly diminishing returns for serial computer architecture performance with increasing logic gates beyond the levels used in VLSI today. The predicted future performance for electronic computers as shown in the Figure 1 is for full utilization of the parallel pipes. The general purpose computing performance of these future processors using parallel super-scalar architectures could improve at a much slower rate than the peak speeds, as the average performance may no longer track the peak serial speed performance. The Semiconductor Industry Association Roadmap predicts the clock rates of these processors will not exceed 1 GHz by the year 2010.<sup>2</sup>

## 2.3 Using optics to advance the technology.

Optics has the capability of dramatically improving this fundamental computer performance via the reduction of capacitance and intrinsic high bandwidth communications. Yet optical devices have not replaced silicon VLSI to date. The reason is very simple. The optical devices to date have not had significantly greater performance with equal computing capability and similarly low manufacturing cost. A number of papers and books in optical computing<sup>3,4</sup> document the great efforts spent to obtain higher performance with optics on a particular component of the computer system. In some cases this optical computing effort has been successful, but at an extreme cost penalty for manufacture and laser supply. The approach taken here is to simply use the same manufacturing techniques that have been successful for silicon electronics and apply them to optics.<sup>5</sup> The individual digital logic components are improved in speed and power by direct optical connections at the gate level. Electronic logic gates in production today have propagation delays in the low 10's of picoseconds in low fanout ring oscillators. But as fanouts are added and wires become longer, the logic gate delays rapidly rise up into many 100s of picoseconds. This phenomenon has been observed with all electronics technologies from Si BiCMOS to GaAs HEMTs. The reason is straightforward. For example, a wire with an oxide and metal width twice the oxide thickness ( $d_2 = w/2$ ) has a capacitance of 30 fF/mm independent of linewidth (see Fig. 2). In practice, the capacitance is 100s of fF/mm because of the thin oxides desired. Since typical digital circuits work with several volts and sub-milliamp currents, the natural resistance is several thousand ohms. Charging a mm length wire then takes 100s of picoseconds, independent of linewidth. A typical fanout for logic is three, and the size of electronic circuits are now exceeding one centimeter. This places serious restrictions on clock speed for logic with electronic wiring. With removal of the capacitance in the fanout logic gates and wiring by using optics, the fundamental electronic logic can reach its natural speed below 10 psecs. Furthermore, the power dissipation in electronics also arises from the charging of these capacitors and is similarly reduced with the use of optical connections. Very Large Scale Integrated Optics (VLSIO) provides high bandwidth interconnections using optical waveguides as transmission lines directly connected to the logic gates.

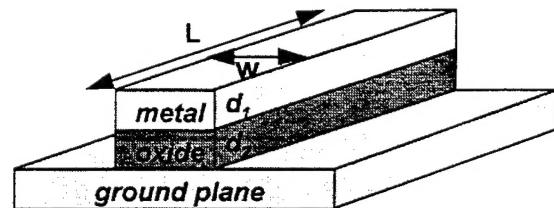


Figure 2. A typical electrical wire with greater than 30 fF/mm capacitance.

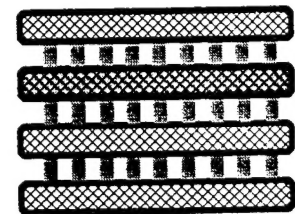


Figure 3. Three dimensional optical coupling between circuits with two dimensional VLSIO wiring.



The manufacture of these components can be done with standard photolithography methods. Many efforts are being made to replace the interface pins used in electronic packaging with optics. It is possible to improve the nanosecond chip collection speed down to the 100s of picosecond on-chip speed. The problem is that silicon is not an optical emitter and only poorly performs other optical functions. So the effort of connecting silicon to optical devices has replaced the effort of connection to an external pin. Which technique is best is very much an engineering function. In contrast, optical connection at the gate level has very fundamental advantages for optics which electronics has difficulty surmounting, practically guaranteeing the migration of computers to optical circuitry at some point in time.

### **3. VERY LARGE SCALE INTEGRATED OPTICS (VLSIO)**

#### **3.1 Integrating optics advances with the production advances of electronics.**

The VLSIO approach also has additional fundamental advantages in manufacture and packaging over electronics. With optics, the logic circuits can be distributed over a number of lower device density chips, but stacked upon each other and connected by lens arrays (see Fig. 3). Packaging with an array of diffractive lenses is lower cost than wire bonding to pins as the chip packaging is nearly complete upon fabrication. A logic chip simply needs to be stacked on top of another chip to be coupled as illustrated in Figure 3. The surface connector array can yield over 10,000 connections per square centimeter, each with a terahertz bandwidth. Massive low cost connectors improve usability of chips with lower component count and ease yield problems. Use of high performance AlGaAs semiconductors has been thwarted in electronic systems by an unfortunate combination of low yield and speed loss in the connectors. The ease of reassembly of optically interconnected stacks allows independent redesign of various components of the computer for improved architectures, rapid prototyping, and design repairs. The greater surface area of a three dimensional stack also allows better cooling of the devices. The lower density of components allows use of lower cost manufacturing techniques. With the reduced requirements of 1 to 3 micrometer linewidths, customized generation of unique hardware could be performed via post-processing in shops similar to photo-processors today. Unique hardware architecture could be acquired much as each user today acquires highly unique program environments and software assortments. With low cost distributed production, billion dollar capital plants are replaced by large numbers of vendors providing high performance customized architectures.

#### **3.2 Integrated optics versus free space approaches.**

Although optical computing in the last two decades has classically used optics to image between arrays of logic, the approach taken here is more like that of standard VLSI electronics. The interconnections are between logic gates on a planar surface. But the connections with Very Large Scale Integrated Optics (VLSIO) use waveguides which have the properties of transmission lines rather than load lines used in today's electronics. Transmission lines require greater attention to reflect off imperfections and impedance matching (or reflectionless absorption at the intended receiver in the case of optics). Transmission lines naturally provide the highest speed transmission for a given length. The optical waveguide as a transmission line also removes capacitance as discussed before. The use of waveguide transmission lines rather than the classical imaging approach of optical computing has several advantages.<sup>5</sup> The average connection distance is 100 to 1000 times shorter using waveguides rather than lenses, reducing propagation delays.<sup>5</sup> The reduced propagation delays are essential to retain the speed advantages of optics in serial computing. The manufacture of waveguides can be performed using the proven photolithographic techniques that created the electronics revolution. In contrast, imaging systems require numerous expensive optical elements be reproduced for each processor. In photolithography, the sophistication of the expensive optics at today's technology maximum resolution are used to project onto the patterned surface. The optics are then released to regenerate a new wiring pattern, often on the very same semiconductor surface. This amortization of the expensive capital plant over millions of processors is what makes computers cheap while the factory is very expensive. Non-replicating optical imaging systems are contradictory to this manufacturing principle. Furthermore, the use of waveguides to wire components allows greater complexity than the million or so isolated pixels allowed with today's lenses. The lens systems also image homogeneously. So more complex signal routing required in any computer architecture, must be created by repeatedly splitting and recombining the image field in various parts. The repeated splitting with various combinations further expands the expensive optics requirements. Finally, components connected by waveguides can be placed at larger separations, not limited by the lens field of

view. The temperature tolerance of the optical components has been a serious limitation in working devices and is easier to control with lower density components spread over several chips.<sup>5</sup> In spite of these strong advantages, very little work is being conducted on VLSIO systems, most likely because of the extreme difficulty of the design of the necessary components and the primitive level of integrated optics.

### 3.3 Ultra High Confinement (UHC) waveguides.

The idea of integrating the optical components onto a single chip was first suggested by S. E. Miller.<sup>6</sup> In spite of the offered promise of high density integration of optical components, two-dimensional lateral connectivity to date has nowhere approached that of VLSI electronics. The obstacle has been the incapability of guiding light with strong dielectric confinement due to the rapid increase in scattering with dielectric ratio. This scattering increases as a square of the difference in dielectric constant between guide and cladding, requiring the dielectric constants to remain within 1% of each other for a typical waveguide.<sup>7</sup>

This requirement has caused the thickness of a typical waveguide to be larger than the free-space wavelength.<sup>8</sup> This larger dimension was also welcomed considering the fabrication capabilities at the time. The practical problem of scattering can be solved by the use of mid-infrared light because the scattering losses drop with wavelength to the third power.<sup>9,10</sup> Ultra High Confinement (UHC) wave-guides can be created with a high refractive index ratio between cladding and guide. Ultra High Confinement is defined here as confinement of light in a waveguide with an effective cross-section less than a tenth of a squared free-space wavelength or a resonator volume less than a cubic free-space wavelength (see Fig. 4). Because of the high confinement, a full vector field analysis of the mode is essential for accuracy. A practical implementation of an UHC waveguide in the mid-infrared region uses Ge with refractive index 4.0 on GaAs with refractive index 3.27.<sup>11</sup> The Ge waveguide can be deposited on top of GaAs substrate via UHV E-Beam evaporation (see the next paper in this conference proceeding).<sup>11</sup> Both the materials have excellent infrared and thermal properties and have almost perfect lattice matching. Any active material can be grown on the GaAs substrate before the Ge evaporation and interact with the strong fields at the Ge/GaAs boundary. An entirely new class of physical devices using the intersubband transition can be used for this mid-infrared interaction. The physical phenomena include lasing, modulation, detectors, second harmonic generation and other nonlinear interactions.<sup>12</sup> The Ge/GaAs UHC waveguide geometry can scale to the near-infrared as lithography resolution improves to  $0.1\mu\text{m}$  with the use of GaAs

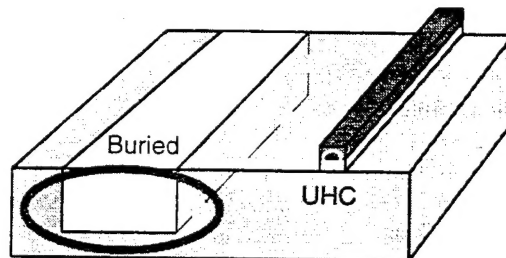


Figure 4. Note UHC waveguides have a mode area 20 times smaller than the typical buried waveguide.

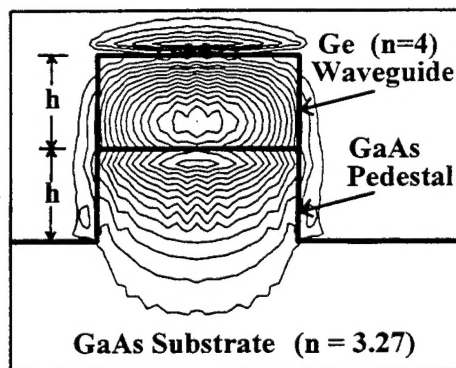


Figure 5. An UHC pedestal waveguide with vertical mode component.

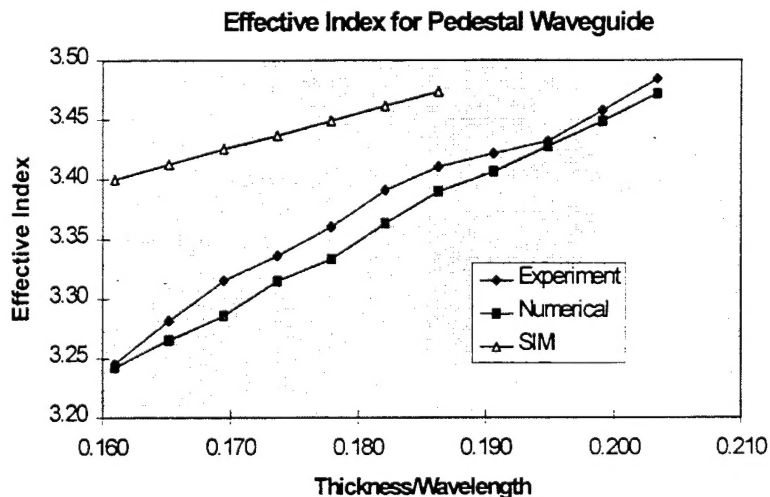
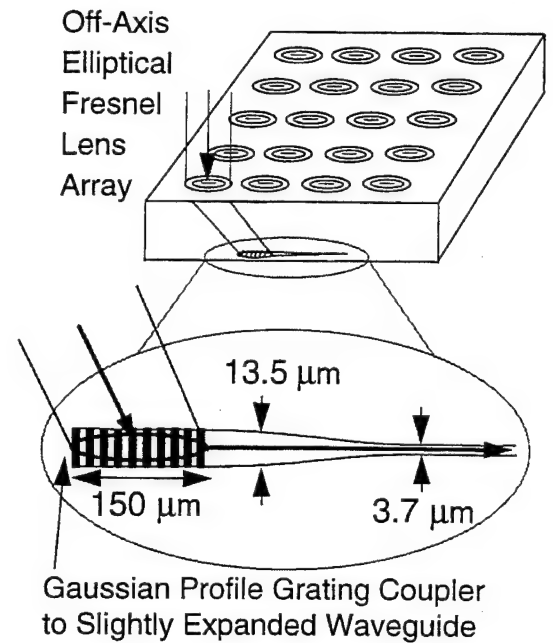


Figure 6. Theory (Spectral Index Method), Experimental (microwave), and Numerical (FEM) results for effective index. Note the numerical modeling and experiment agree well, but not the theory.

with refractive index 3.6 as the waveguide on AIAs with refractive index 2.9.

### 3.4 Analysis of UHC waveguides.

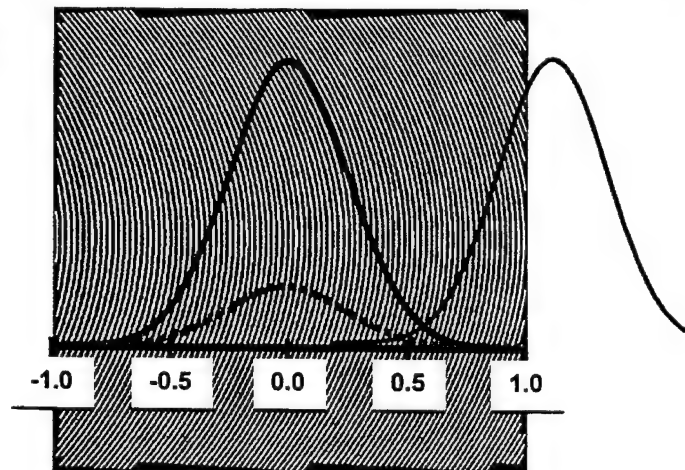
Using the numerical analysis and microwave experiments we show that a large index ratio confines the light into a waveguide with dimensions a small fraction of the wavelength of light. Figure 5 shows the electric field profile for the vector component in the vertical direction. This vector mode profile was derived numerically using a custom finite element method (FEM) time domain program.<sup>13</sup> An approximate mode was generated and propagated down the guide until steady state was achieved. The effective index of the mode was calculated from the linear phase shift with distance. This procedure was repeated for several ratios of waveguide height to free space wavelength. To test the new UHC waveguide properties, we conducted microwave scaled experiments. This scale testing is much in analogy to that of wind tunnel tests for airplanes. We purchase dielectric materials in the 4 GHz microwave region that have the same dielectric constant as Ge (4.0) and GaAs (3.27) with an accuracy of better than 3%. The microwave scaled waveguides are machined to a size of  $h=12.7$  mm and width of 25.4 mm. Propagation experiments similar to that of the numerical are performed on the real microwave guides and the effective index measured. Note the size scaling of the waveguide to the microwave for the optics is a perfect scaling. No effects are partially scaled. The results are shown in Fig. 6. These results show good confinement ( $n_{\text{eff}} > 3.27$ ) when  $h/\lambda$  is greater than 0.170. In practice, we use  $h/\lambda$  between 2.0 and 2.1.



**Figure 7.** Coupling to UHC waveguide with a normal incidence  $120 \mu\text{m}$  diameter beam.

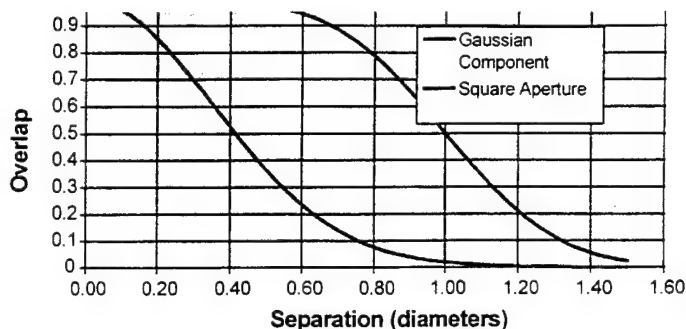
### 3.5 Coupling into UHC waveguides.

Coupling into the UHC waveguides has been a major practical obstacle to their fabrication and testing. The buried waveguide mode has relative large size of one to three free space wavelengths that allows direct output from a cleaved edge. The UHC waveguide has a dimension that is about 0.2 by 0.3 free space wavelengths, which does not allow efficient coupling to air from the edge of the waveguide. A technique has been developed for robust coupling to these guides for a round Gaussian beam normal to the GaAs wafer surface. This coupling involves several steps, each using a sophisticated optical element. First, the UHC waveguide is adiabatically tapered from  $3.7 \mu\text{m}$  wide rectangular mode to  $13.5 \mu\text{m}$  wide slab mode over a distance of  $40 \mu\text{m}$ . This wide mode is then scattered at a 21 degree angle into the substrate with a nonuniform, but periodic grating coupler. The teeth of the coupler are monotonically increased in scattering strength so as to radiate a Gaussian intensity profile with a diameter of  $120 \mu\text{m}$ . The angle in the substrate is greater than the total internal reflection angle to ensure no radiation to the air side of the coupler. The highly elliptical spot size is then coupled to a round Gaussian profile beam with a diameter of  $120 \mu\text{m}$  by use of an aspheric off-axis elliptical four level Fresnel lens on the back side of the substrate. All critical coupling steps of the interconnection are done at the lithography stage. The through-wafer



**Figure 8.** Off-Axis Elliptical Diffraction Lens with misaligned Gaussian beam shown as a function of beam diameter.

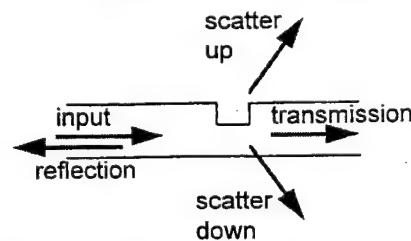
alignment of the lens to the Gaussian coupler needs to be better than  $1.0\text{ }\mu\text{m}$  to ensure  $< 10\%$  loss in efficiency. This alignment is performed by using a round Fresnel lens to burn a small alignment spot on the opposite side of the wafer with a  $\text{CO}_2$  laser. Once the lens array is fabricated, the wafer has a good tolerance to misalignment. The angle of the input beam must be within 10 milliradians for high efficiency. However, semiconductor wafers are flat to within  $10\text{ }\mu\text{m}$  and most large particles are less than  $20\text{ }\mu\text{m}$  so a stacked cm square wafer will naturally be aligned to within 1 milliradian. The narrow 10 milliradian acceptance angle in two dimensions filters out unwanted scattered light. The  $120\text{ }\mu\text{m}$  diameter mid-infrared beam can propagate 2 mm in free space without diffracting, allowing wide tolerance in spacing of the chip stack. The lateral misalignment of the Gaussian beam causes loss of efficiency. The large size of the diffraction lens improves the tolerance to lateral misalignment and particles on the surface. However, too large a lens reduces the number of couplers per square centimeter. A good compromise is the  $120\text{ }\mu\text{m}$  diameter beam and a  $180\text{ }\mu\text{m}$  diameter lens allowing  $3000\text{ couplers/cm}^2$  to be created. The diffraction lens has less acceptance area than indicated by its aperture. This is because the coupling to the UHC waveguide requires single mode input. A lateral misalignment only couples to the extent the beam it has a component with the centered Gaussian beam (see Fig. 9). Note a  $20\text{ }\mu\text{m}$  lateral misalignment for the  $120\text{ }\mu\text{m}$  diameter beam causes a 10% loss in coupling. However, a noise source at the correct angle and beam profile but separated by  $120\text{ }\mu\text{m}$  only has a 3% coupling. A wrong angle or beam profile typical of noise has very low coupling. The strong single mode nature of this coupler naturally excludes noise effectively creating a pipe for the light. However, the tolerance of this coupler is well adjusted to that angle and position which are reasonable allowable for stacks of wafers.



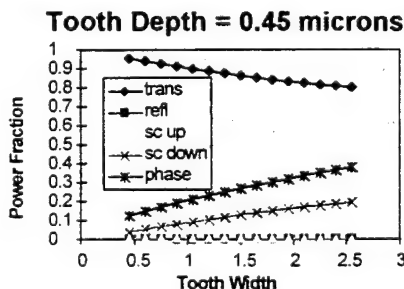
**Figure 9.** Loss of coupling with lateral misalignment of the diffraction lens. The lens aperture is actually that of the

### 3.6 The non-uniform grating coupler to a waveguide from a Gaussian beam.

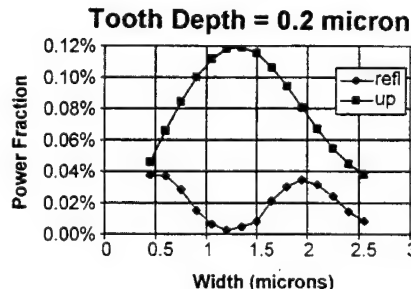
The line focus Gaussian beam must couple efficiently into the waveguide. Normally, a uniform periodic grating coupler limits the efficiency of the coupling to less than 80% at best, with actual couplers much lower. The large  $10\text{ }\mu\text{m}$  wavelength allows non-periodic grating couplers to radiate a profile more of a Gaussian than a decaying exponential for improved efficiency. A preferred method would keep the tooth depth constant and vary the width that is easy to fabricate with standard lithography. After extensive effort, we found that the very large coupling variation needed required at least two etch depths for sufficient range of tooth coupling. The current design uses 33 teeth with a  $4.5\text{ }\mu\text{m}$  period and two masks with etch depths of  $0.2\text{ }\mu\text{m}$  and  $0.45\text{ }\mu\text{m}$ . The design started with the measure of single tooth scattering coefficients for transmission, reflection, and scatter, including phase shifts for a number of different teeth. The transmission phase variation was used to vary the period slightly to get a uniform scattered phase. After completion of the design from these single tooth parameters, the total Gaussian couplers as then modeled with the Finite Element Method in two dimensions for a slab waveguide. The output of this coupler X as measured for Gaussian diameter and overlap. The final design had a Gaussian overlap into the desired beam



**Figure 10.** Single tooth model for calculating coupling coefficients.



**Figure 11.** Single tooth transmission, phase shift, and scatter to the substrate for a  $0.45\text{ }\mu\text{m}$  depth.



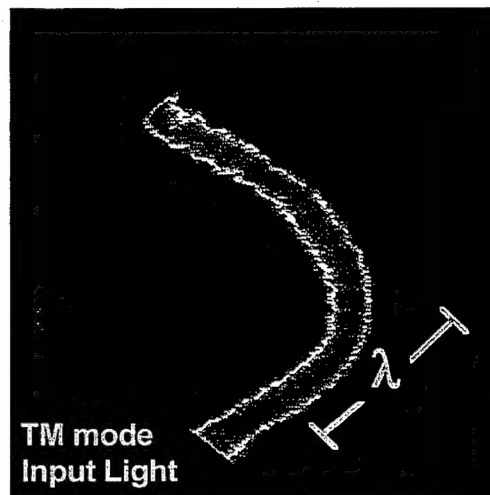
**Figure 12.** Single tooth reflection and scatter to air expanded for the  $0.2\text{ }\mu\text{m}$  deep tooth.

of 85%. The losses were from scatter to air, backwards scatter down the waveguide, backwards scatter at -21 degrees into the substrate, uncoupled transmission, in the waveguide, and non-Gaussian components of the scattered beam. Each of these scatter losses are less than a few percent. The coupler attempted to use only a tooth width near that of a half wave in the waveguide. This was because the  $1.5\text{ }\mu\text{m}$  width was easy to fabricate and the single tooth has minimum back scatter down the waveguide for this width (see Figures 11 and 12). The taper has a 98% efficiency as modeled by the Finite Element Method.

### 3.7 High density routing of UHC waveguides.

One of the greatest benefits of the high index of refraction is the ability to create waveguide bends with a radius of less than one free space wavelength. This tight bend allows creation of dense components for VLSIO (see Fig. 13). Both FEM modeling and microwave experiments show that a right angle bend with a radius of  $7.5\text{ }\mu\text{m}$  for  $10\text{ }\mu\text{m}$  light has a 90% efficiency for single mode transmission. A high density circuit would need an corner efficiency greater than 95%. Further improvements may be difficult, and not needed as the active components are capable of restoring the signals.

The other element needed for high density routing is a low loss 'cross-over' element, that allows optical wires to cross one another in the same signal plane. Electrical wires cannot perform this unique function as they will short their signals. The availability of a good cross-over element could reduce the number signal planes, especially for the lower density logic created. Crossovers with loss as low as 1 dB per wire have been created, but more design work is needed here. A preferred crossover would have less than 3% loss per wire crossed, and less than -50 dB cross-talk. Again, active components are capable of restoring the signal loss to some extent. These goals are anticipated to be achievable.



**Figure 13.** A cross section of the field of a pedestal waveguide mode propagating around a  $7.5\text{ }\mu\text{m}$  radius bend.

### 3.8 Ultra-compact resonators with UHC waveguides.

The UHC waveguide has several advantages in opto-electronic device improvement due to its small size. The UHC waveguides are capable of creating resonators with volumes less than one tenth of a cubic free space wavelength. This is 1000 times smaller than VCSELs. The 20 times smaller beam diameter improves gain and other optical properties by a similar factor. The capacitance of the devices is also much reduced, improving the bandwidth of optoelectronic devices by more than a factor of 10 over buried waveguides, nearing 1 THz in frequency response. For example, modulators created with UHC resonators for the mid-infrared are predicted to have 3 fF capacitance and less than 7 fJ time-power product. As the UHC waveguides are scaled 10-fold smaller to the near-infrared with improved lithography, these numbers are lowered 100 fold. It should be noted however, that 1.0 micrometer resolution lithography is barely adequate for the sophisticated elements discussed here, even though our wavelength is 10 microns. For instance, the tooth width shown in Figure 12 must vary from  $0.9$  to  $1.8\text{ }\mu\text{m}$  with  $0.1\text{ }\mu\text{m}$  precision. This capability is just possible with  $1.0\text{ }\mu\text{m}$  linewidth lithography, tenfold smaller than the free space wavelength. Similar requirements are seen for most all our components. As such, near-infrared use of UHC concepts will not be viable until the availability of  $0.1\text{ }\mu\text{m}$  linewidth lithography. However, highly useful components can be created in the mid-infrared today which will develop the UHC integrated optics.



#### 4. SUMMARY

This development of UHC waveguides for VLSIO is at its beginning, but showing good promise for providing optical components with the same density as current electronics. Furthermore, it is possible using the components illustrated here to create fully three dimensional computer systems with high connectivity and reasonable tolerances for fabrication and packaging with position and angle. We also show that UHC waveguides can connect in a two dimensional plane at compact sizes which allow very much improved opto-electronic performance, leading to true terahertz technologies.

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